Experiment No. 06

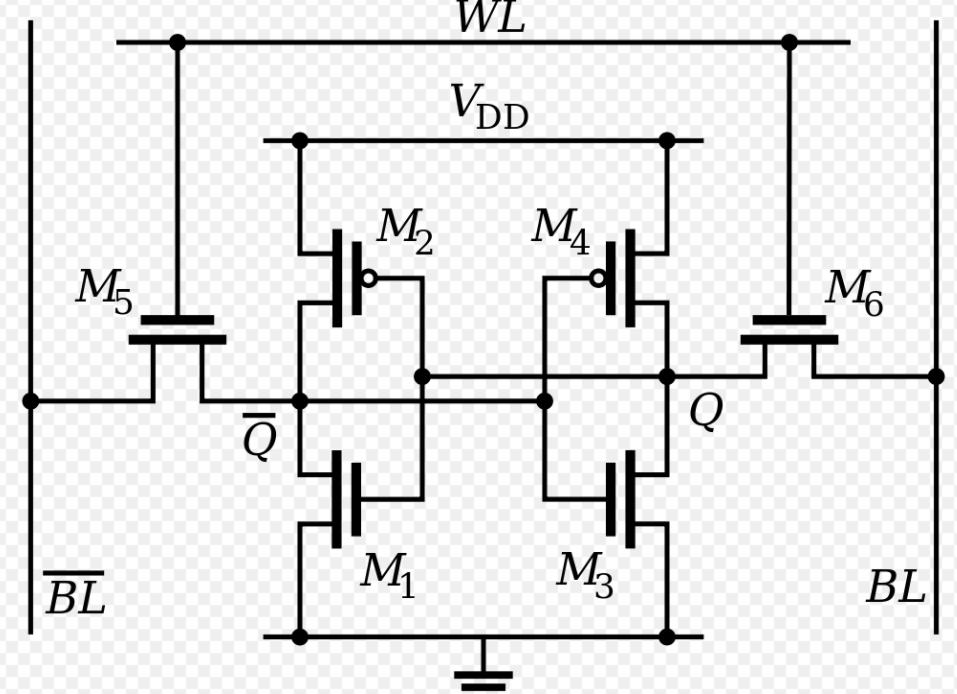
**Schematic of 6T SRAM**

**OBJECTIVE:** To simulate the schematic of 6T SRAM.

**SOFTWARE**: LT Spice

**THEORY:**

A typical SRAM cell is made up of six [MOSFETs](https://en.wikipedia.org/wiki/MOSFET). Each [bit](https://en.wikipedia.org/wiki/Bit) in an SRAM is stored on four [transistors](https://en.wikipedia.org/wiki/Transistor) (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors serve to control the access to a storage cell during read and write operations.

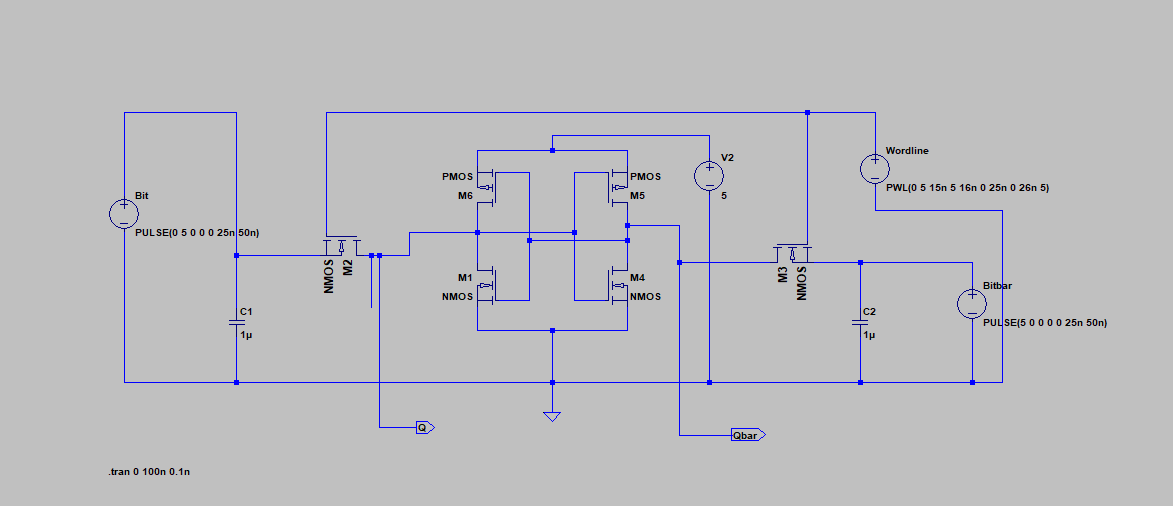
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The cell is enabled by the word line (WL in figure) which controls the two *access* transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve [noise margins](https://en.wikipedia.org/wiki/Noise_margin).

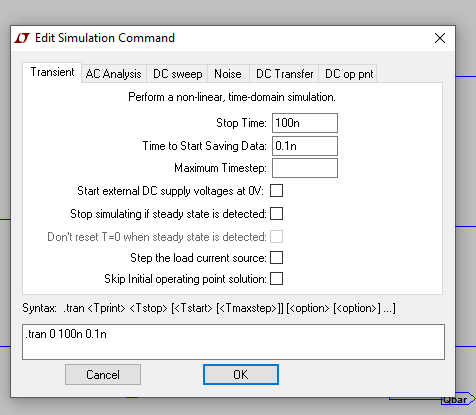
**PROCEDURE:**

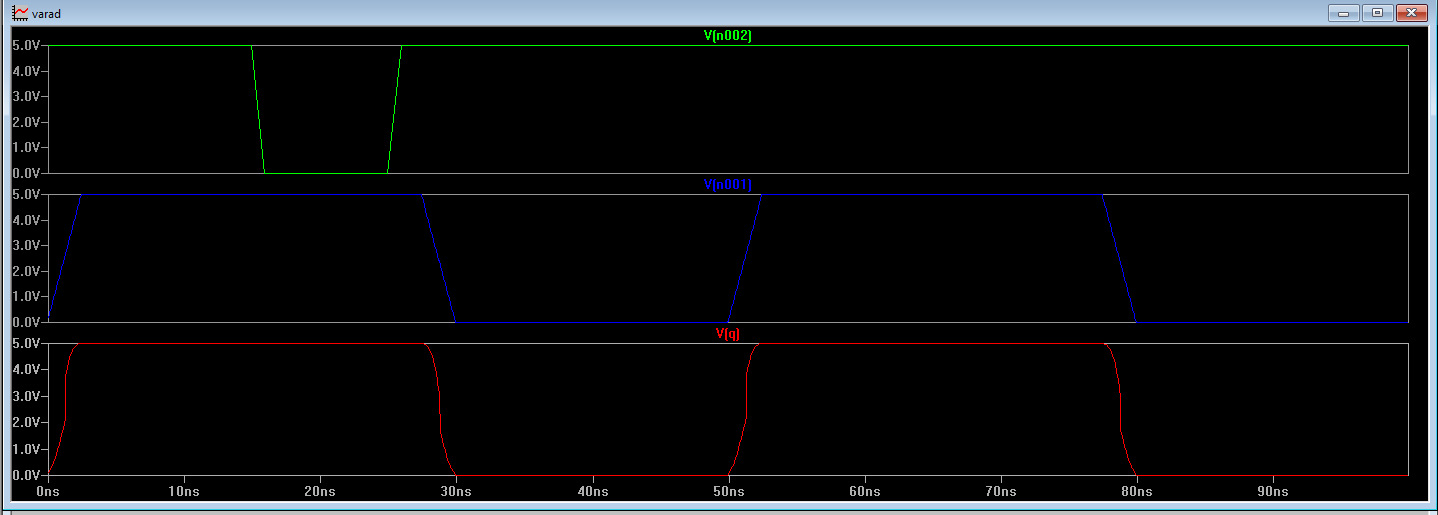
1. Open LT spice
2. In **Files** Menu---click on **new** **Schematic**---Give name to schematic
3. Go to **Components**---Select each required component----do connections.
4. Select Transient analysis. Assign voltage to each voltage node.
5. Simulate the schematic

**OUTPUT:**

**Circuit Diagram**

**Waveform :**





**CONCLUSION:**

**The Schematic of ST ram in Ltspice was performed successfully. The output was generated and verified in Ltspice.**